REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration of this application is requested. Claims 1-15 are now pending with claim 1 being independent. Claims 1 and 2 have been amended.

Claim 1 has been amended in response to the Examiner's claim objection on page 2 of the Office Action mailed February 11, 2004.

The specification has been amended to correct minor errors and other informalities. No new matter has been introduced.

Claim 1 has been amended in response to the Examiner's rejections under 35 U.S.C. § 103(a).

As amended, claim 1 describes a data transfer system including a plurality of first bus devices, at least one first bus device is a first bus data supplying device capable of supplying data. At least one first bus device is a first bus data receiving device capable of receiving data and at least one first bus device is a first bus master device capable of requesting and controlling data transfer. A first data bus is connected to each of the plurality of first bus devices and capable of transferring data from a first bus data supplying device to a first bus data receiving device under control of a first bus master device. The data transfer system further includes a plurality of second bus devices, at least one second bus device is a second bus data supplying device capable of supplying data. At least one second bus device is a second bus data receiving device capable of receiving data and at least one second bus device is a second bus master device capable of requesting and controlling data transfer. A second data bus is connected to each of the plurality of second bus devices and capable of transferring data from a second bus data supplying device to a second bus data receiving device under control of a second bus master device. The data transfer system includes a bus bridge connected to the first data bus and the second data bus, the bus bridge capable of supplying data to the first bus, receiving data from the first bus, supplying data to the second bus, receiving data from said second bus. The bus bridge is not capable of controlling data transfer on the first bus and capable of controlling data transfer on the second bus. The bus bridge includes an address first-in-first-out memory having a predetermined number of entries including an input connected to the first bus and an output

connected to the second bus. The bus bridge also includes a data first-in-first-out memory having the predetermined number of entries including an input connected to the first bus and an output connected to the second bus, wherein the bus bridge does not allow a read request over the second bus until address first-in-first-out memory and data first-in-first-out memory are empty.

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Reiss et al. (6,571,308) in view of Rooney (6,601,118). Applicants request reconsideration and withdrawal of these rejections because neither Reiss or Rooney describes or suggests the bus bridge not allowing a read request over the second bus until address first-in-first-out memory and data first-in-first-out memory are empty.

Reiss shows in Figure 1 and describes in the Abstract and columns 5-6 an expansion module 12 for a Handspring Visor 11 that includes a multi-master AMBA Advanced System Bus (ASB) 15. Optionally, an Arm7 processor 17 is attached to this bus via an Arm7 to ASB interface 33 as one master. The Springboard bus (SBB) 14 of the Visor 11 is coupled to the ASB bus 15 via a Springboard-to-ASB-bus bridge 30. This bridge comprises a protocol translator 31 and a second Arm7 to ASB interface 33. The protocol translator translates bi-directionally between the Springboard bus protocol and the Arm7TDMI protocol. The translator includes an interface 35 to the Springboard bus and a state machine 37. The state machine coordinates data transfers between the buses. The state machine also monitors signals indicating when each of the buses begins to treat a data transfer as complete so that the data transfer can be validated or flagged as an error condition. Reiss does not describe or suggest the bus bridge not allowing a read request over the second bus (ASB bus) until address first-in-first-out memory and data first-in-first-out memory are empty. As the Examiner admits on page 4 of the Office Action, Reiss does not describe or suggest an address first-in-first-out memory buffer and a data first-in-first-out memory buffer included in the bus bridge interface. Accordingly, Reiss makes no reference to the bus bridge not allowing a read request over the second bus until address first-in-first-out memory and data first-in-first-out memory are empty.

The bus bridge not allowing a read request over the second bus until the address first-in-first-out memory and data first-in-first-out memory are empty provides several advantages. In particular, the bus bridge not allowing read requests until the memory buffers are empty creates

timing conditions to prevent read-after-write (RAW) errors due to potential delays induced in bus synchronization and arbitration. RAW errors may result in incorrect program execution because data in the devices connected by the bus bridge are not the same.

Rooney describes in the Abstract a system for dynamically allocating buffers between devices in a computer system. The system uses matched sets of bi-directional buffers to control data flow between the processor bus and the computer bus. The dynamic buffer allocation system allows simultaneous data transfer from the processor to the buffers, and from the buffers to the peripheral bus. In Rooney, as shown in Figure 1, a bridge circuit 11 couples a processor device 7 on a processor bus 9 to peripheral devices on a peripheral bus 17. The bridge circuit 11 includes address and data buffers 15 that control data flow between the processor and peripheral devices on the peripheral bus 17. Rooney in column 3 teaches that the Intel Pentium® Pro processor may perform a "deferred" data read from the PCI bus. After the data is read from the PCI device, it is sent to a deferred data handling circuit before being sent to the processor bus and processor. A deferred data handler keeps track of the outstanding deferred data reads and notifies the Pentium® Pro processor when a deferred data read from a PCI device is available. Rooney does not describe or suggest the bus bridge not allowing a read request over the second bus until address first-in-first-out memory and data first-in-first-out memory are empty. For at least these reasons, Applicants respectfully submit that claims 1-6 are patentable over the Reiss and Rooney references.

Claims 7-15 depend from independent claim 1. Accordingly, Applicants requests reconsideration and withdrawal of the rejections for claims 7-15 for the reasons discussed above with respect to claim 1.

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brooks (6,532,511) in view of Rooney (6,601,118). Applicants request reconsideration and withdrawal of these rejections because, as admitted by the Examiner in page 6 of the Office Action, Brooks does not disclose an address FIFO buffer and a data FIFO buffer. Thus, Brooks fails to remedy the failure of Rooney to describe or suggest the bus bridge not allowing a read request over the second bus until address first-in-first-out memory and data first-in-first-out memory are empty.

Brooks describes in the Abstract and shows in Figures 1 and 2 an electronic bridging device for transferring electronic data between a first device attached to a system bus and a

peripheral device attached to a peripheral bus using a bridging circuit. A DMA controller comprises a system bus interface circuit for connecting the DMA controller to the system bus, a peripheral bus interface circuit for connecting the DMA controller to the peripheral bus, a data transfer request circuit for receiving data transfer requests from devices attached to the peripheral bus, and control logic circuit for controlling the operation of DMA data transfer operations. Brooks makes no reference to the bus bridging circuit not allowing a read request over the second bus until address first-in-first-out memory and data first-in-first-out memory are empty. For at least these reasons, Applicants respectfully submit that claims 1-6 are patentable over Brooks and Rooney.

Claims 7-15 depend from independent claim 1. Accordingly, Applicants request reconsideration and withdrawal of the rejections for claims 7-15 over the Brooks and Rooney references for the reasons discussed above with respect to claim 1.

The Examiner on pages 6 and 7 of the Office Action in rejecting claims 7-15 under 35 U.S.C. § 103(a) "takes Official Notice that the use of a full or empty bit, set by the bridge to indicate whether the address/data buffers are full or empty; and to generate an interrupt of the processor in the bridge when the address/data buffers are full or empty, is old and well-known, and using a full or empty bit, set by the bridge in Brook for the purpose of indicating whether the address/data buffers are full or empty; and to generate an interrupt of the processor in the bridge when the address/data buffers are full or empty, only involves ordinary skill in the art." Applicants respectfully challenge the Official Notice and request supportive documents teaching the elements of claims 7-15. In particular, use of a bus bridge setting a predetermined buffer full/empty bit of the at least one control register when the address first-in-first-out memory and the data first-in-first-out memory are full/empty; the bus bridge generating an interrupt of the central processing unit when the address first-in-first-out memory and the data first-in-first-out memory are full/empty; and the bus bridge setting a predetermined buffer full bit of the at least one control register when an entry in the address first-in-first-out memory and the data first-in-first-out memory has been overwritten are not common knowledge or well known in the art. These elements are not common knowledge or well known in the art because in data transfer systems some external control other than the bus bridge such as a processor sets control bits and generates interrupts. Furthermore, the elements officially noticed are not readily verifiable since

they are not supported by the Reiss, Rooney or Brooks references of record and are in fact contradicted by the Rooney reference. Rooney as shown in Figure 1 and described in columns 2 and 3 teaches dynamically allocating address and data buffer entries during periods of high data transfer to solve the problem of address and data buffers being full so that entries containing data or addresses in the buffers are not overwritten. As such, under 37 CFR 1.104(c)(2), Applicants respectfully challenge the Official Notice and request supportive documents teaching the elements of claims 7-15.

In view of these remarks and amendments, Applicants submit that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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